ICmic
IC MICROSYSTEMS

12/10/8-Bit Low Power Voltage Output Quad DACs With Parallel Interface

FEATURES

- 12/10/8-Bit Quad DAC s
- Ultra-Low Power Consumption
- Guaranteed Monotonic
- Wide Voltage Swing Output Buffer
- Parallel Interface with Double Buffered Inputs
- Shutdown Capability

APPLICATION

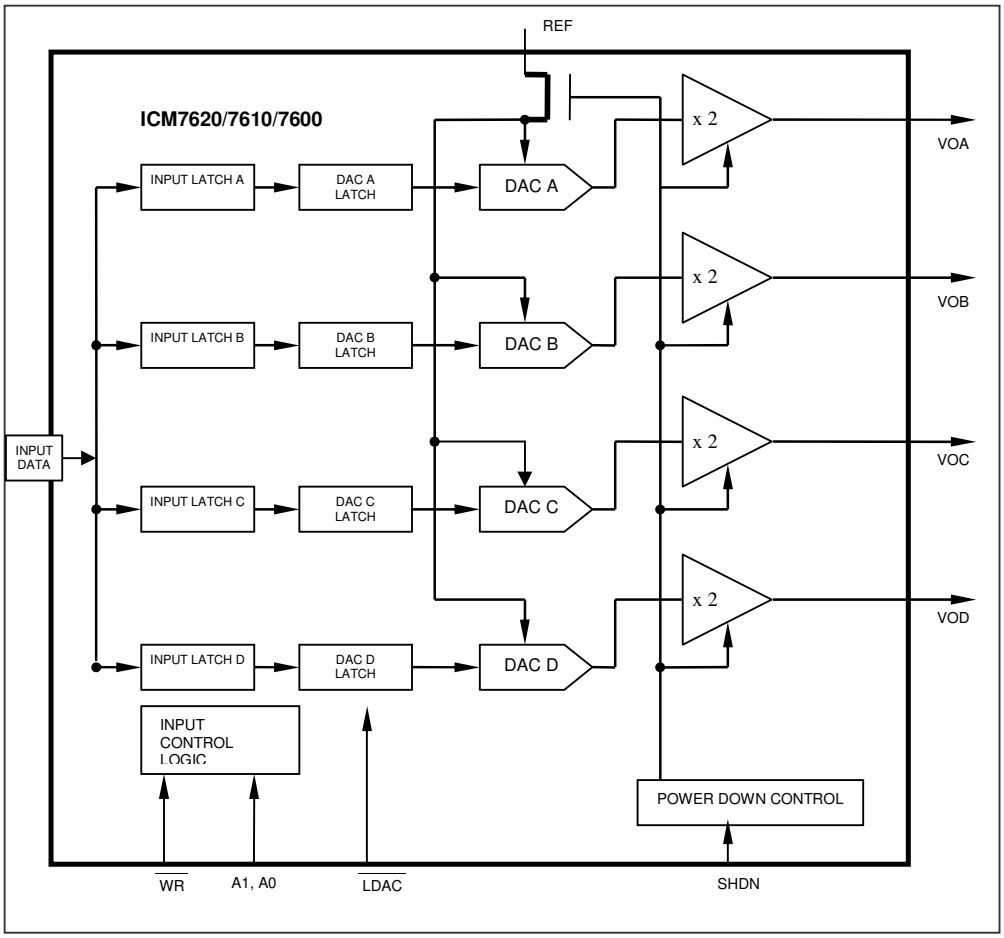
- Battery-Powered Applications
- Industrial Process Control
- Digital Gain and Offset Adjustment

The ICM7620, ICM7610 and ICM7600 are 12-Bit, 10-Bit and 8-Bit Voltage Output, Low Power, Quad DACs respectively, with guaranteed monotonic behavior. These DACs are available in 20 and 24 Lead TSSOP packages. The input interface for the devices is 12 (ICM7620), 10 (ICM7610) and 8 (ICM7600) bit parallel interface. They operate from a single supply which can range from 2.7V to 5.5V.

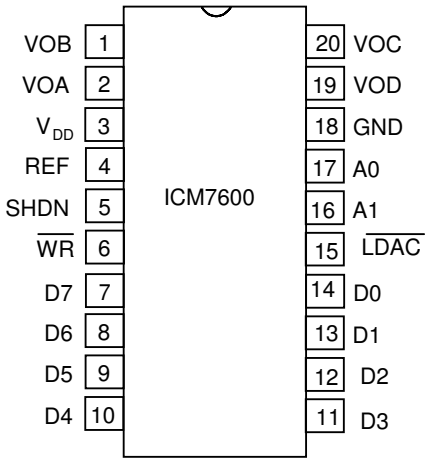
These DACs also offer a shutdown feature. When active, this will shutdown all DACs and would disconnect the REF input from the DACs internally. The supply current is reduced to below 10 µA in shutdown mode.

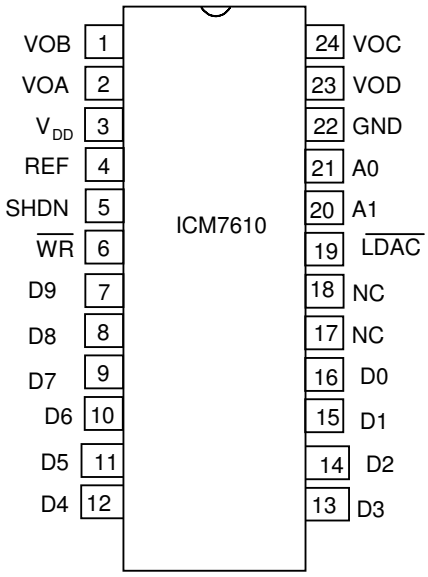
OVERVIEW

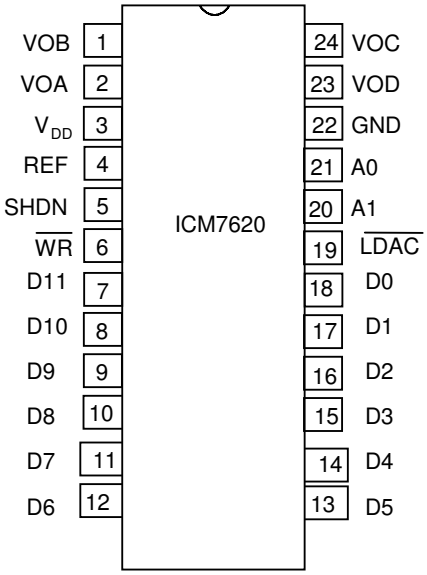
BLOCK DIAGRAM



PACKAGES (20 LEAD – ICM7600, 24 LEAD TSSOP – ICM7610, ICM7620)







PIN DESCRIPTION (ICM7600)

Pin	Name	I/O	Description
1	VOB	O	DAC B Output Voltage
2	VOA	O	DAC A Output Voltage
3	VDD	I	Supply Voltage
4	REF	I	Reference Voltage Input to All DAC
5	SHDN	I	Shutdown (Active high)
6	$\overline{WR}$	I	Write Input (active low). Used to load input into input latch.
7-14	D7-D0	I	Data Inputs
15	$\overline{LDAC}$	I	Load DAC Input (active low).
16	A1	I	DAC Address Select Bit (MSB)
17	A0	I	DAC Address Select Bit (LSB)
18	GND	I	Ground
19	VOD	O	DAC D Output Voltage
20	VOC	O	DAC C Output Voltage

PIN DESCRIPTION (ICM7610)

Pin	Name	I/O	Description
1	VOB	O	DAC B Output Voltage
2	VOA	O	DAC A Output Voltage
3	VDD	I	Supply Voltage
4	REF	I	Reference Voltage Input to All DAC
5	SHDN	I	Shutdown (Active high)
6	$\overline{WR}$	I	Write Input (active low). Used to load input into input latch.
17-18	NC		No connection
7-16	D9-D0	I	Data Inputs
19	$\overline{LDAC}$	I	Load DAC Input (active low).
20	A1	I	DAC Address Select Bit (MSB)
21	A0	I	DAC Address Select Bit (LSB)
22	GND	I	Ground
23	VOD	O	DAC D Output Voltage
24	VOC	O	DAC C Output Voltage

PIN DESCRIPTION (ICM7620)

Pin	Name	I/O	Description
1	VOB	O	DAC B Output Voltage
2	VOA	O	DAC A Output Voltage
3	VDD	I	Supply Voltage
4	REF	I	Reference Voltage Input to All DAC
5	SHDN	I	Shutdown (Active high)
6	$\overline{WR}$	I	Write Input (active low). Used to load input into input latch.
7-18	D11-D0	I	Data Inputs
19	$\overline{LDAC}$	I	Load DAC Input (active low).
20	A1	I	DAC Address Select Bit (MSB)
21	A0	I	DAC Address Select Bit (LSB)
22	GND	I	Ground
23	VOD	O	DAC D Output Voltage
24	VOC	O	DAC C Output Voltage

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
I_{IN}	Input Current	+/- 25.0	mA
$V_{IN\_}$	Digital Input Voltage (D0~D11, A1, A0 , $\overline{WR}$, $\overline{LDAC}$)	-0.3 to 7.0	V
V_{IN_REF}	Reference Input Voltage	-0.3 to 7.0	V
T_{STG}	Storage Temperature	-65 to +150	^oC
T_{SOL}	Soldering Temperature	300	^oC

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ORDERING INFORMATION

Part	Operating Temperature Range	Package
ICM7620	-40 ^oC to 85 ^oC	24-Lead TSSOP
ICM7610	-40 ^oC to 85 ^oC	24-Lead TSSOP
ICM7600	-40 ^oC to 85 ^oC	20-Lead TSSOP

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, V_{OUT} unloaded; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
ICM7620						
N	Resolution		12			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.4	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		4.0	±12.0	LSB
ICM7610						
N	Resolution		10			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.1	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		1.0	±3.0	LSB
ICM7600						
N	Resolution		8			Bits
DNL	Differential Nonlinearity	(Notes 1 & 3)		0.05	±1.0	LSB
INL	Integral Nonlinearity	(Notes 1 & 3)		0.25	±0.75	LSB
STATIC ACCURACY						
GE	Gain Error				±1.0	% of FS
OE	Offset Error				±35	mV
POWER REQUIREMENTS						
V_{DD}	Supply Voltage		2.7	5	5.5	V
I_{DD}	Supply Current	Full Scale at VDD=5..5		300	700	µA
	Supply Current	Full Scale at VDD=3.6		200	550	µA
	Supply Current	In Shutdown		5	20	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{OUT} unloaded; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Vout	Output Voltage Range	(Notes 2 & 3)	0		V_{DD}	V
VO_{SC}	Short Circuit Current			60	150	mA
	Output Line Regulation	V_{DD}=2.7V to 5.5V	-3.0	0.4	3.0	mV/V
LOGIC INPUTS						
V_{IH}	Digital Input High	(Note 2)	0.5xV_{DD}			V
V_{IL}	Digital Input Low	(Note 2)			0.2xV_{DD}	V
	Digital Input Leakage	(Note 2)			5	µA

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, V_{OUT} unloaded; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SR	Slew Rate			0.33		V/µs
	Settling Time			12		µs
	Mid-scale Transition Glitch Energy			40		nV-S

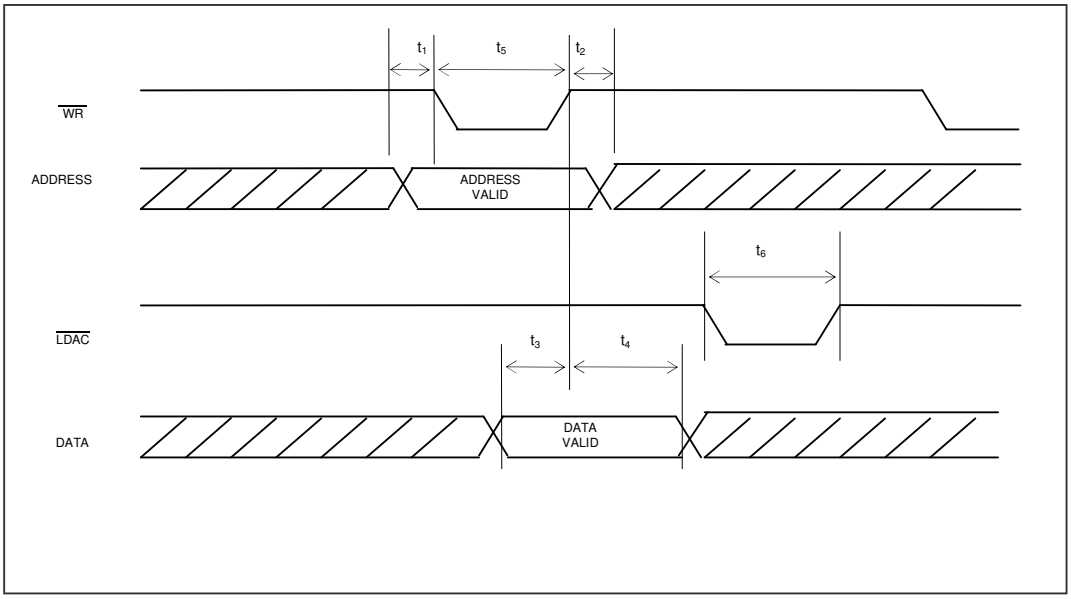
TIMING CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_1	Address to $\overline{WR}$ Setup Time	(Note 2)	5			ns
t_2	Address to $\overline{WR}$ Hold Time	(Note 2)	0			ns
t_3	Data to $\overline{WR}$ Setup Time	(Note 2)	20			ns
t_4	Data to $\overline{WR}$ Hold Time	(Note 2)	0			ns
t_5	$\overline{WR}$ Pulse Width	(Note 2)	15			ns
t_6	$\overline{LDAC}$ Pulse Width	(Note 2)	15			ns

Note 1: Linearity is defined from code 110 to 3990 (ICM7620)
Linearity is defined from code 16 to 1023 (ICM7610)
Linearity is defined from code 4 to 255 (ICM7600)
Note 2: Guaranteed by design; not tested in production
Note 3: See Applications Information

TIMING AND OPERATION DIAGRAM



$\overline{LDAC}$	$\overline{WR}$	A1	A0	LATCH STATE
1	1	X	X	Input and DAC data latched
1	0	0	0	Input Latch transparent – DAC A
0	1	X	X	DAC Latch transparent – All DACs
0	0	0	0	DAC latch of All DACs transparent and DAC A input latch transparent
1	0	0	1	Input Latch transparent – DAC B
1	0	1	0	Input Latch transparent – DAC C
1	0	1	1	Input Latch transparent – DAC D

Table 1. Address Table

DETAILED DESCRIPTION

The ICM7620 is a 12-bit voltage output Quad DAC. The ICM7610 is the 10-bit version of this family and the ICM7600 is the 8-bit version. These devices have a parallel interface and each DAC has a double buffered input. This family of DACs has a guaranteed monotonic behavior. The operating supply range is from 2.7V to 5.5V.

Reference Input

The reference input accepts positive DC and AC signals. The voltage at REFIN sets the full-scale output voltage of all the DACs. The reference input voltage range is from 0 to VDD-1.5V. The impedance at this pin is nominally about 40 K Ω. Each DACs output amplifier is configured in a gain of 2 configuration. This means that the full-scale output of each DAC will be 2x V_{REF}. To determine the output voltage for any code, use the following equation.

$$V_{OUT} = 2 \times (V_{REF} \times (D / (2^n)))$$

Where D is the numeric value of DAC's decimal input code, V_{REF} is the reference voltage and n is number of bits, i.e. 12 for ICM7620, 10 for ICM7610 and 8 for ICM7600.

Output Buffer Amplifier

The Quad DAC has 4 output amplifiers connected in a gain of 2 configuration. These amplifiers have a wide output voltage swing. The actual swing of the output amplifiers will be limited by offset error and gain error. See the Applications Information Section for a more detailed discussion.

The output amplifier can drive a load of 2.0 K Ω to V_{DD} or GND in parallel with a 500 pF load capacitance and has a full-scale typical settling time of 8 µs.

Input Logic

This quad DAC family uses a standard straight parallel interface where D0 is the LSB and D11 is the MSB for the ICM7620, D9 is the MSB for the ICM7610 and D7 is the MSB for the ICM7600. Each DAC has its own double buffered input with an input latch and a DAC latch. Each DAC will go the voltage output that corresponds to the digital data that is stored in its DAC latch.
The $\overline{WR}$ Input (active low), controls the input latch data and the $\overline{LDAC}$ Input (active low) updates the DAC latches (Table 1). Please refer to the Timing Diagram for more detail. The address inputs (A1, A0) control DAC addressing (Table 1).

Power-Down Mode

These parts offer shutdown capability to the user by means of the SHDN pin. When this pin is forced high all the DACs power down and the REF input goes into high impedance state. The total current consumption will go down to below 10 µA in power down mode. The data is stored in the latches during power down and the DACs will power up in the previous state when SHDN is driven back to logic low.

Power-On Reset

There is a power-on reset on board that will clear the contents of all the latches to all 0s on power-up and the DAC voltage output will go to ground.

APPLICATIONS INFORMATION

Power Supply Bypassing and Layout Considerations

As in any precision circuit, careful consideration has to be given to layout of the supply and ground. The return path from the GND to the supply ground should be short with low impedance. Using a ground plane would be ideal. The supply should have some bypassing on it. A 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic with a low ESR can be used. Ideally these would be placed as close as possible to the device. Avoid crossing digital and analog signals, specially the reference, or running them close to each other.

Output Swing Limitations

The ideal rail-to-rail DAC would swing from GND to V_{DD}. However, offset and gain error limit this ability. Figure 1 illustrates how a negative offset error will affect the output. The output will limit close to ground since this is single supply part, resulting in a dead-band area. As a larger input is loaded into the DAC the output will eventually rise above ground. This is why the linearity is specified for a starting code greater than zero.

Figure 2 illustrates how a gain error or positive offset error will affect the output when it is close to V_{DD}. A positive gain error or positive offset will cause the output to be limited to the positive supply voltage resulting in a dead-band of codes close to full-scale.

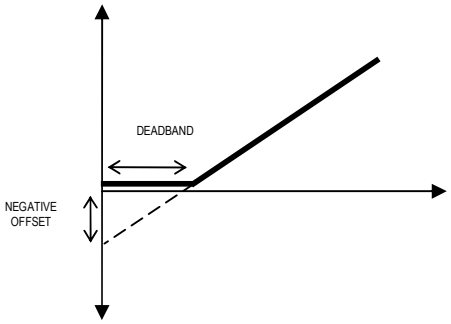


Figure 1. Effect of Negative Offset

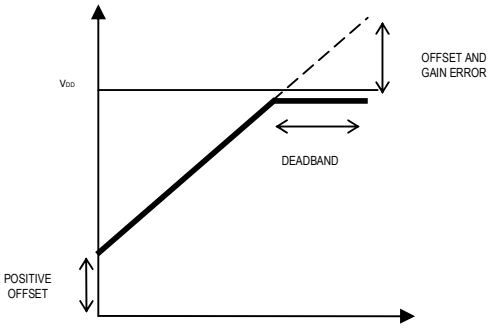
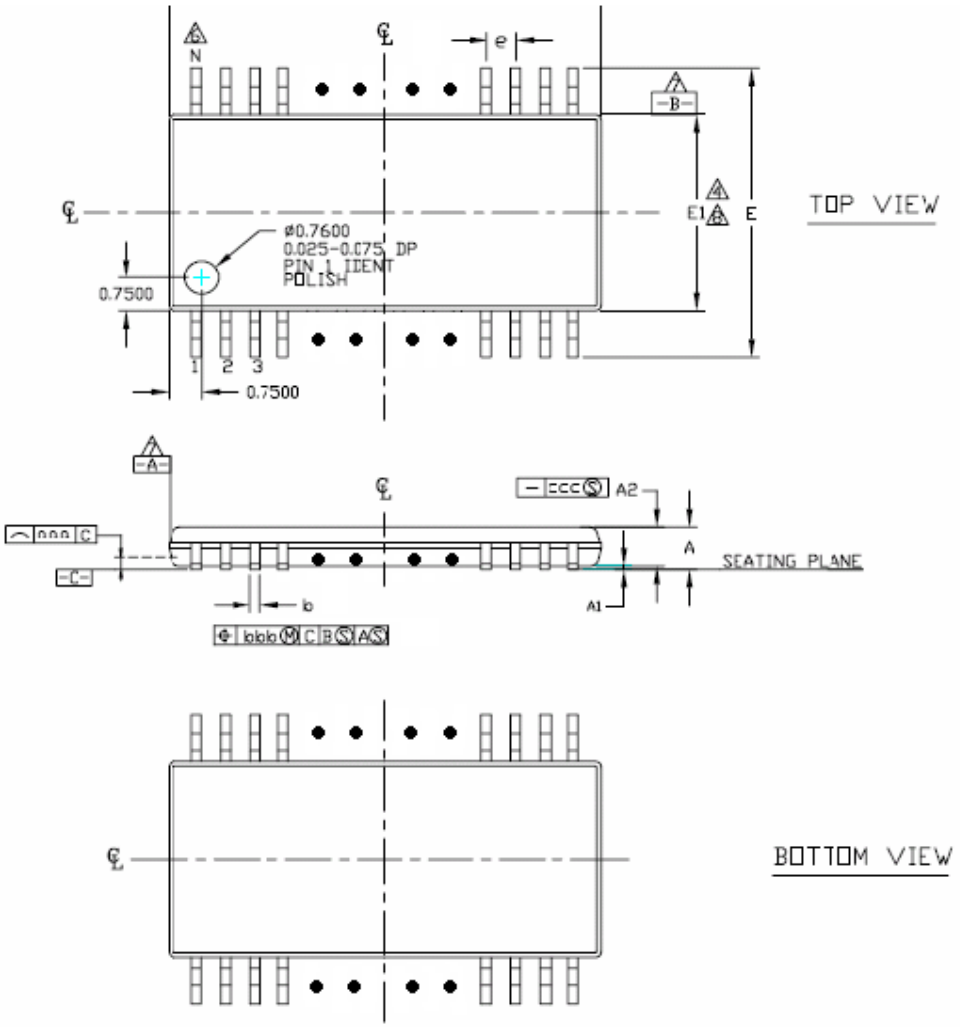
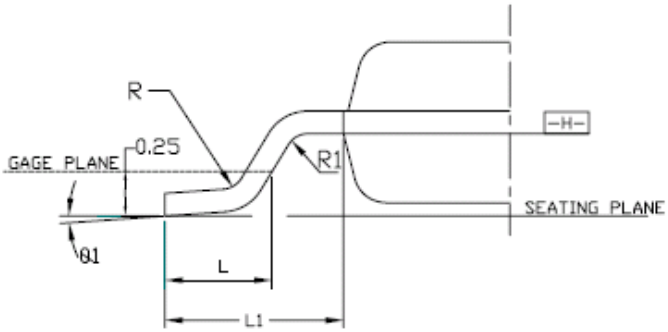


Figure 2. Effect of Gain Error and Positive Offset

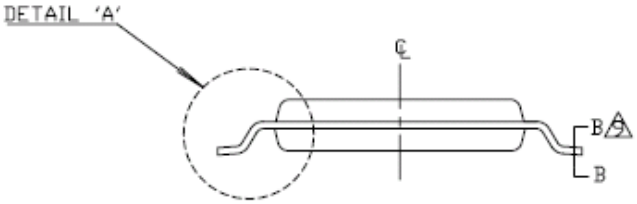
PACKAGE INFORMATION

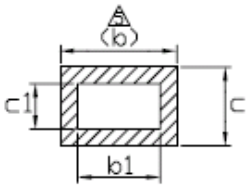
20 Lead TSSOP, 24 Lead TSSOP





DETAIL 'A'





DETAIL 'B-B'

SYMBOL	20L TSSOP		
	MIN	NOM.	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	0.90	1.05
D	6.4	6.5	6.6
E1	4.3	4.4	4.5
E	6.2	6.4	6.6
L	0.45	0.60	0.75
R	0.09	—	—
R1	0.09	—	—
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
θ1	0	—	8
L1	1.0 REF		
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.20		
e	0.65 BSC		
N	20		
Ref.	Jedec MO-153 Issue C Variation AC		

SYMBOL	24L TSSOP		
	MIN	NOM.	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	0.90	1.05
D	7.7	7.8	7.9
E1	4.3	4.4	4.5
E	6.2	6.4	6.6
L	0.45	0.60	0.75
R	0.09	—	—
R1	0.09	—	—
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
θ1	0	—	8
L1	1.0 REF		
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.20		
e	0.65 BSC		
N	24		
Ref.	Jedec MO-153 Issue C Variation AD		

ORDERING INFORMATION

ICM76X0 P G

Device
2 - ICM7620
1 - ICM7610
0 - ICM7600

G = RoHS Compliant Lead-Free package.
Blank = Standard package. Non lead-free.

Package
T = TSSOP Package